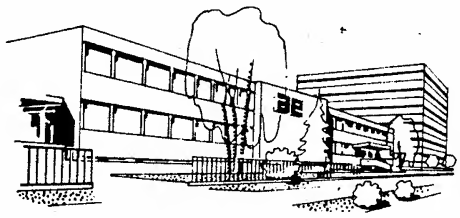
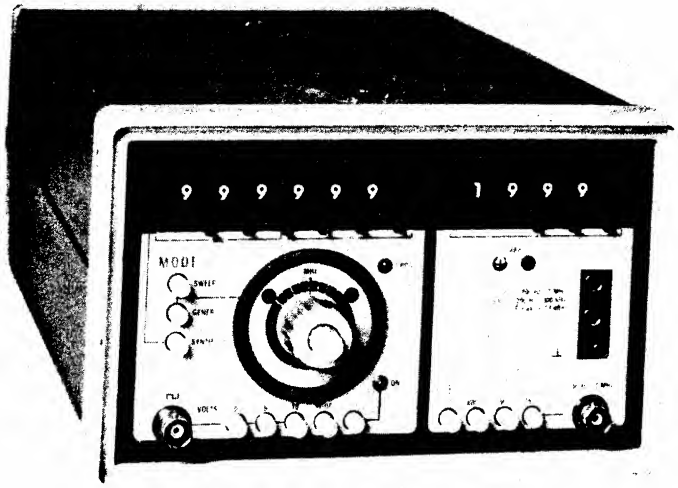
ADRET *ELECTRONIQUE* ®





LEVEL GENERATOR
FREQUENCY SYNTHESIZER
50Hz_1MHz

2230A

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SUMMARY

SUMMARY

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CHAPTER I

FUNCTIONAL DESCRIPTION

I FUNCTIONAL DESCRIPTION

The model 2230A is a programmable frequency and level generator which covers the 50 Hz to 1 MHz range with 1 Hz resolution.

The output frequency can be controlled according to four operating modes : digital setting by six lever/indicator switches, remote programming in parallel BCD code or through the IEEE bus, analogical setting by two verniers with graduated scale, frequency sweep by external signal.

Four output signals are simultaneously available :

- A main output with pushbutton selectable impedance : 75 Ω coaxial, 150 Ω balanced, 600 Ω balanced, or low-impedance balanced (key 0 Ω).
- An auxiliary output with Z < 1 Ω impedance.
- A square-wave output with 5 V or 10 V amplitude.
- A tracking output delivering a signal with 4 MHz offset with respect to the dialled or programmed frequency.

The output level of the main signal ranges from + 19.99 dBm to - 69.99 dBm for the 75 Ω impedance, and from + 13 dBm to - 69.99 dBm for the impedances with balanced output. The level setting is directly displayed in dBm into the selected impedance (75 Ω, 150 Ω or 600 Ω). Besides, an Inhibition key permits to suppress the output signal without switching off the instrument.

The frequency and level remote programming is achieved either in parallel BCD code (option 010), or through the IEEE bus (option 020). Besides, the output level regulation may be performed with two distinct time constants, which allows to reduce the level settling time to less than 10 ms for frequencies above 10 kHz.

CHAPTER II

SPECIFICATIONS

II SPECIFICATIONS

FREQUENCY

Main output :

- 75 Ω impedance : 50 Hz* to 1 MHz
- 150 Ω impedance : 200 Hz to 1 MHz
- 600 Ω impedance : 200 Hz to 300 kHz
- 0 Ω/150 Ω impedance : 200 Hz to 1 MHz
- 0 Ω/600 Ω impedance : 200 Hz to 300 kHz

Tracking output with 4 MHz offset : 4 MHz to 5 MHz

Square wave output : 50 Hz* to 1 MHz

Auxiliary output : 50 Hz* to 1 MHz

Resolution : 1 Hz

Selection : 6 lever/indicator switches

Stability : $\pm$ 3.10^{-6}/24 h, from / 10°C to + 40°C.

* *This instrument can be used down to 10 Hz on the 75 Ω, square-wave and auxiliary outputs with some restrictions in the specifications.*

EXTERNAL REFERENCE

Substitution of the external reference for the built-in Master Oscillator.

Frequency : 5 MHz

Level : 220 mVrms to 1 Vrms/50 Ω

REFERENCE OUTPUT

Frequency : 1 MHz

Level : approximately 500 mVrms/50 Ω

FREQUENCY CONTINUOUS ADJUSTMENT

Frequency range : as for digital setting.

Frequency adjustment : by two verniers with graduated scale and by switches controlling the 1 Hz, 10 Hz and 100 Hz increments.

Dial accuracy : $\pm$ 5 % of full scale.

In this operating mode, the output frequency can be compared to the digital setting of the switches controlling the 1 kHz, 10 kHz and 100 kHz increments, thanks to a frequency comparator with LED display.

FREQUENCY SWEEP

Frequency range : same as for digital setting.

Sweep : By ± 5 V external signal.

- Input impedance : 100 kΩ
- Sensitivity : 10 mVpeak for 1 kHz deviation
- Linearity : ± 10 %
- Bandwidth :

  DC to 500 Hz for ± 5 kHz deviation
  DC to 50 Hz for ± 50 kHz deviation
  DC to 5 Hz for ± 500 kHz deviation

In this operating mode, the center frequency around which the sweep is performed depends on the two verniers with graduated scale, as also on the switches controlling the 1 Hz, 10 Hz and 100 Hz increments.

Besides, the output frequency can be compared to the digital setting of the switches controlling the 1 kHz, 10 kHz and 100 kHz increments, thanks to a frequency comparator with LED display.

OUTPUT LEVEL

Several signals are simultaneously available :

- The main signal, delivered on the front panel with 0 Ω, 75 Ω, 150 Ω or 600 Ω impedance selected by pushbutton.
- A square-wave output, delivered on the front panel.
- A tracking signal with 4 MHz frequency offset, delivered on the rear panel.
- An auxiliary signal with very low output impedance, delivered on the rear panel.

Main output :

The main output is available with five pushbutton selectable impedances : 75 Ω coaxial, 150 Ω balanced, 600 Ω balanced, 0 Ω/150 Ω balanced (Z < 5 Ω) and 0 Ω/600 Ω balanced (Z < 20 Ω).

Level display : in dBm by four lever/indicator switches, with sign display by light-emitting diodes.

Resolution : 0.01 dB

Dynamic range : 89.98 dB for 75 Ω impedance and 82.99 dB for other impedances.

Output level :

- 75 Ω impedance : + 19.99 dBm to - 69.99 dBm/75 Ω
- 150 Ω impedance : + 13 dBm to - 69.99 dBm/150 Ω
- 600 Ω impedance : + 13 dBm to - 69.99 dBm/600 Ω
- 0 Ω/150 Ω impedance :

Electromotive force equal to that of 150 Ω impedance, that is 3.46 Vrms (+ 13 dBm setting) to 245 µVrms (- 69.99 dBm setting).

Maximum output current : 30 mA rms

- 0 Ω/600 Ω impedance :

Electromotive force equal to that of 600 Ω impedance, that is 6.92 Vrms (+ 13 dBm setting) to 490 µVrms (- 69.99 dBm setting).

Maximum output current : 15 mA rms

Accuracy at 0 dBm for a 10 kHz frequency : ± 0.2 dB

Output level flatness :

- 75 Ω impedance : + 0.05 dB from 50 Hz to 1 MHz
- 150 Ω and 0 Ω/150 Ω impedances : ± 0.05 dB from 200 Hz to 200 kHz
  ± 0.1 dB from 200 kHz to 620 kHz
  ± 0.2 dB from 620 kHz to 1 MHz
- 600 Ω and 0 Ω/600 Ω impedances : ± 0.05 dB from 200 Hz to 110 kHz
  ± 0.3 dB from 110 kHz to 300 kHz

Reflection loss :

- 75 Ω impedance : + 0 dBm to + 20 dBm : - 35 dB from 50 Hz to 1 MHz
  - 0 dBm to - 69.99 dBm : - 45 dB from 50 Hz to 1 MHz
- 150 Ω impedance : - 35 dB from 200 Hz to 200 kHz
  - 30 dB from 200 kHz to 1 MHz
- 600 Ω impedance : - 35 dB from 200 Hz to 110 kHz
  - 30 dB from 110 kHz to 300 kHz

Signal unbalance :

- 150 Ω impedance : - 50 dB from 200 Hz to 620 kHz
- 600 Ω impedance : - 50 dB from 200 Hz to 110 kHz

Attenuator accuracy :

- 0.01 dB steps : ± 0.005 dB per step, ± 0.01 dB maximum error
- 0.1 dB steps : ± 0.01 dB per step, ± 0.02 dB maximum error
- 1 dB steps : ± 0.03 dB per step, ± 0.05 dB maximum error
- 10 dB steps : ± 0.1 dB per step, ± 0.2 dB maximum error from 0 dBm to - 60 dBm.

Tracking output :

Level : + 6 dBm/75 Ω ± 2 dB

Square-wave output :

- Amplitude : 0 V, 5 V or 10 V typical
- Rise time : < 300 ns
- Fall time : < 100 ns

Auxiliary output :

- Impedance : Z < 1 Ω from 50 Hz to 500 kHz
  Z < 1.5 Ω from 500 kHz to 1 MHz
- Level : + 19.99 dBm/75 Ω to 0 dBm/75 Ω, depending on main output level.
- Output current : 50 mA rms maximum

Protection against short-circuits.

- Maximum capacitive loading : 4.7 nF from 50 Hz to 500 kHz
  1 nF from 500 kHz to 1 MHz
- Output level flatness : ± 0.5 dB from 50 Hz to 200 Hz
  ± 0.3 dB from 200 Hz to 1 MHz

SPECTRAL PURITY

Harmonic signals :

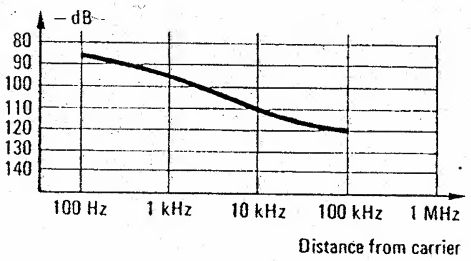
Main output (+ 10 dBm output level) :

- 75 Ω impedance : - 45 dB from 50 Hz to 300 Hz
  - 55 dB from 300 Hz to 1 MHz
- 150 Ω and 0 Ω/150 Ω impedances : - 50 dB from 200 Hz to 1 MHz
- 600 Ω and 0 Ω/600 Ω impedances : - 50 dB from 200 Hz to 300 kHz

Auxiliary output (+ 10 dBm/75 Ω output level) : - 40 dB from 50 Hz to 300 Hz
- 50 dB from 300 Hz to 1 MHz

Nonharmonic signals : - 60 dB for all outputs

Phase-noise in a 1 Hz band :



REMOTE PROGRAMMING

Remote programming of the instrument is achieved either in parallel BCD code (option 010) or through the IEEE bus (option 020).

Parallel BCD programming (option 010) :

- TTL compatible positive logic. "0" logic level : 0 V to + 0.8 V
  "1" logic level : + 2 V to + 5 V
- Parallel BCD code.

IEEE bus programming (option 020) :
Compatible with IEEE standard 488-1975.

SH0 : the instrument never emits data.

AH1 : the instrument accepts data.

T0-TE0 : the instrument is not a Talker.

L1-LE0 : the instrument is a basic Listener which recognizes its own address, does not get disaddressed on reception of the corresponding Talker address, and may be permanently addressed.

SR0 : the instrument has no Service Request capability.

PP0 : the instrument does not respond to Parallel Poll.

RL1 : the Remote mode is controlled through the IEEE bus.

DC1 : the instrument has complete Device Clear capability.

DT1 : the instrument has complete Device Trigger capability.

Frequency programming :

- Resolution : 1 Hz
- Settling time : 10^3 Hz to 10^5 Hz steps : 7 ms
  10^0 Hz to 10^2 Hz steps : 10 ms.

Level programming :

- Resolution : 0.01 dB
- Settling time : 10 dB steps between - 0 dBm and - 60 dBm : 10 ms

Switching between + 0 dBm and + 10 dBm, 1 dB, 0.1 dB and 0.01 dB steps :
5 ms with ALC time constant F > 10 kHz, 800 ms with ALC time constant F < 10 kHz.

Functional mode programming :

- Local/Prog.
- Output level inhibition
- ALC time constant

POWER REQUIREMENTS

Voltage : 115 V or 230 V (± 10 %)
Frequency : 50 Hz to 400 Hz
Consumption : 20 VA

Dimensions :
Height : 140 mm
Width : 200 mm
Overall depth : 352 mm
Adaptable to 19" rack (3 U)

Temperature range :
Operation : 0°C to + 50°C
Storage : - 20°C to + 70°C

Weight : 6 kg

III PRINCIPLE OF OPERATION

III-1 INTRODUCTION

The operation of ADRET synthesizers is based on the indirect frequency synthesis, making use of phase-locked loops composed of a voltage-controlled oscillator, a programmable counter and a phase comparator, as shown in figure III-1.

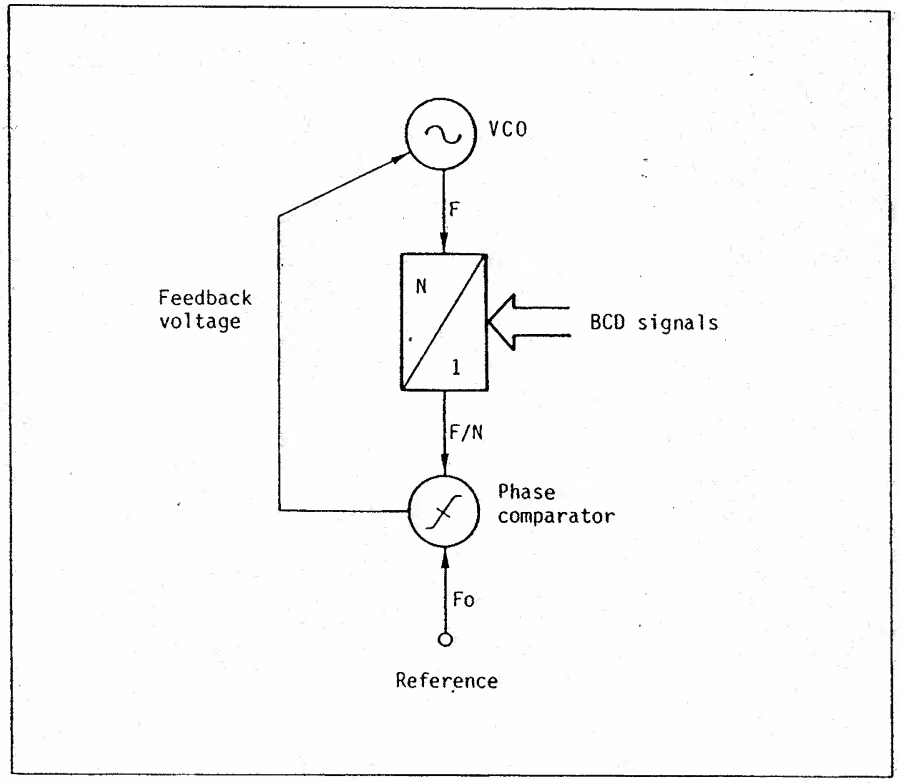


Figure III-1 PHASE-LOCKED LOOP PRINCIPLE

The F frequency delivered by the oscillator is applied to the programmable counter, the N division rate of which is controlled by BCD programming signals. The F/N frequency provided by the programmable counter is then compared to an F_o reference frequency in the phase comparator, which gives a phase-locking voltage allowing to maintain the F frequency of the oscillator equal to N times the F_o reference.

Such a phase-locked loop can thus generate ten different frequencies multiple of F_o when the N division rate of the programmable counter has ten different values.

III-2 PRINCIPLE OF THE 2230A SYNTHESIZER

The general principle of the 2230A synthesizer is represented in plate III-1.

The elaboration of the synthesizer output frequency is achieved through two phase-locked loops : the first loop generates the 10^0 Hz, 10^1 Hz and 10^2 Hz increments of the output frequency, while the second loop generates the 10^3 Hz, 10^4 Hz and 10^5 Hz increments. In the Generator and Sweeper modes, the phase-locking voltage which controls the oscillator of the second loop is replaced by a DC voltage issued from verniers (P1), upon which an external voltage applied to connector (J7) may be superimposed in Sweeper mode.

The mixing of the frequencies elaborated by the two phase-locked loops provides a signal ranging from 4 MHz to 5 MHz in 1 Hz steps, that constitutes the tracking output with 4 MHz offset available on connector (J4). This signal is then heterodyned down in the output mixer with a 4 MHz frequency, which provides a 10 Hz to 1 MHz signal. After amplification, this signal is fed to the shaper delivering the square wave available on connector (J3), to the amplifier of the Z < 1 Ω auxiliary output, and to an attenuator followed with an impedance transformer providing various impedances (75 Ω coaxial, 0 Ω balanced, 150 Ω balanced or 600 Ω balanced) to the main output.

The level of the main output is adjustable from - 69.99 dBm to + 19.99 dBm with 0.01 dB resolution through a digital-to-analog converter which acts upon the ALC loop and varies the level of the 4 MHz signal in 0.01 dB, 0.1 dB and 1 dB steps, whereas the output attenuator provides up to 70 dB attenuation in 10 dB steps.

CHAPTER IV

OPERATING INSTRUCTIONS

IV OPERATING INSTRUCTIONS

IV-1 CONTROLS DESCRIPTION

The various controls and connections on the front and rear panels of the 2230A synthesizer are described in the two following plates :

Plate IV-1 : Front-panel description.
Plate IV-2 : Rear-panel description.

IV-2 INSTALLATION

Connection to mains is achieved on socket (S02) through a standard cord supplied with the instrument. Before applying power, check that mains voltage selector (K8) is on the position corresponding to the mains voltage, remembering that the 115 V and 230 V values admit ± 10 % variation.

The instrument is protected against short-circuits by fuse (F1) of 150 mA nominal value for a 230 V mains voltage, or 300 mA for a 115 V mains voltage.

Switching on the instrument is achieved by pressing key (K1), which lights up indicator (DS1).

IV-3 OUTPUT FREQUENCY

In Local mode, the output frequency can be controlled in three different ways selected by keyboard (K3) : Synthesizer mode, Generator mode, Sweeper mode.

IV-3-1 SYNTHESIZER MODE

In this operating mode, selected by pressing the "SYNTH." key of keyboard (K3), the output frequency is digitally set through lever/indicator switches (K2).

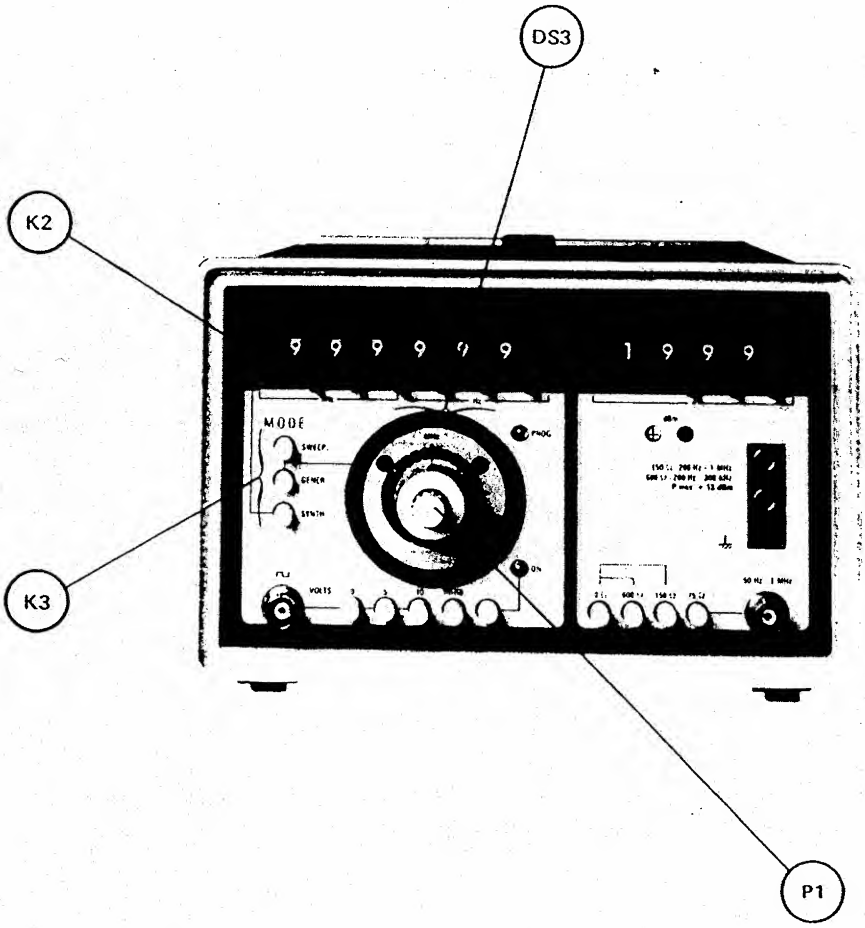
IV-3-2 GENERATOR MODE

This operating mode is obtained by pressing the "GENER." key of keyboard (K3).

The output frequency is determined both by the two verniers (P1) and by the (K2) switches controlling the 1 Hz, 10 Hz and 100 Hz frequency steps, whereas the three other (K2) switches are inhibited.

Two light-emitting diodes (DS3) allow to compare the output frequency to the digital display of switches (K2), this comparison being performed with the three switches controlling the 1 kHz, 10 kHz and 100 kHz frequency steps.

When the output frequency is superior to the digital display of switches (K2), the right-hand LED lights up and the left-hand LED goes out. On the contrary, the left-hand LED lights up and the right-hand LED goes out if the output frequency is inferior to the digital display. When the output frequency is approximately equal to the digital display of switches (K2), a very slow blinking of one LED is observed.



- Press the **GENER.** key of keyboard K3.
- Adjust the output frequency through verniers P1.
- For accurate determination of the output frequency, operate the three K2 switches controlling the 1 kHz, 10 kHz and 100 kHz steps so that one of indicator lights DS3 slowly blinks.
- If necessary, modify the output frequency with the three K2 switches controlling the 1 Hz, 10 Hz and 100 Hz steps.

Figure IV-1 GENERATOR MODE

IV-3-3 SWEEPER MODE

This operating mode, selected by pressing the "SWEEP." key of keyboard (K3), differs from the Generator mode only in the possibility to sweep the output signal around the frequency selected by verniers (P1) and by the (K2) switches controlling the 1 Hz, 10 Hz and 100 Hz frequency steps.

The frequency sweep is achieved by applying an external voltage to connector (J7) whose input sensitivity is 100 kHz per volt. As shown in figure IV-2, the entire frequency range can be swept by a 10 Vp-p signal with a DC offset depending on the setting of verniers (P1).

For instance, if verniers (P1) are set to 0.2 MHz, sweeping the entire frequency range is achieved by applying a signal with 10 Vp-p amplitude centered on + 3 V.

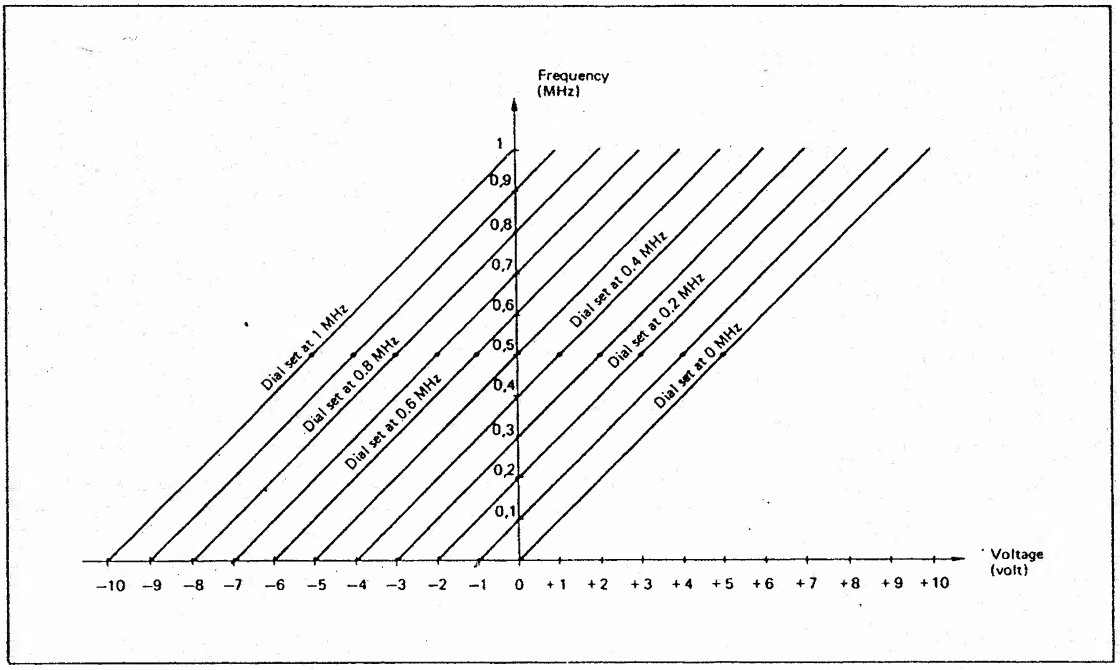


Figure IV-2 OUTPUT FREQUENCY SWEEP

As in the Generator mode, the (DS3) light-emitting diodes allow to compare the output frequency to the digital display of switches (K2), this comparison being performed with the three switches controlling the 1 kHz, 10 kHz and 100 kHz frequency steps.

IV-4 MAIN OUTPUT

Depending on the impedance selected on keyboard (K5), the main output signal is delivered either on coaxial connector (J1) or on balanced connector (J2).

IV-4-1 75 Ω IMPEDANCE

This impedance is selected by pressing the "75 Ω" key of keyboard (K5). The output signal is available on coaxial connector (J1) and the output level is digitally set in dBm/75 Ω through switches (K4), with sign display provided by indicator lights (DS4).

The usable frequency range goes from 10 Hz to 1 MHz, while the output level ranges from + 19.99 dBm (2.735 Vrms/75 Ω) to - 69.99 dBm (86.7 µVrms/75 Ω) with 0.01 dB resolution.

IV-4-2 150 Ω IMPEDANCE

This impedance is selected by pressing the "150 Ω" key of keyboard (K5). The output signal is available on balanced connector (J2) and the output level is digitally set in dBm/150 Ω through switches (K4), with sign display provided by indicator lights (DS4).

The usable frequency range goes from 200 Hz to 1 MHz, while the output level ranges from + 13 dBm (1.730 Vrms/150 Ω) to - 69.99 dBm (122.6 µVrms/150 Ω) with 0.01 dB resolution.

IV-4-3 600 Ω IMPEDANCE

This impedance is selected by pressing the "600 Ω " key of keyboard (K5). The output signal is available on balanced connector (J2) and the output level is digitally set in dBm/600 Ω through switches (K4), with sign display provided by indicator lights (DS4).

The usable frequency range goes from 200 Hz to 300 kHz, while the output level ranges from + 13 dBm (3.460 Vrms/600 Ω) to - 69.99 dBm (245.2 µVrms/600 Ω) with 0.01 dB resolution.

IV-4-4 0 Ω/150 Ω IMPEDANCE

When both the "0 Ω" and "150 Ω" keys are pressed, connector (J2) delivers a signal with less than 5 Ω output impedance. The electromotive force of this signal is equal to that of the signal with 150 Ω output impedance, that is twice the level displayed in dBm/150 Ω by switches (K4) and indicator lights (DS4).

The usable frequency range goes from 200 Hz to 1 MHz, while the electromotive force ranges from 3.46 Vrms (+ 13 dBm/150 Ω display) to 245 µVrms (- 69.99 dBm/150 Ω display) in 0.01 dB steps.

IV-4-5 0 Ω/600 Ω IMPEDANCE

When both the "0Ω" and "600 Ω" keys are pressed, connector (J2) delivers a signal with less than 20 Ω output impedance. The electromotive force of this signal is equal to that of the signal with 600 Ω output impedance, that is twice the level displayed in dBm/600 Ω by switches (K4) and indicator lights (DS4).

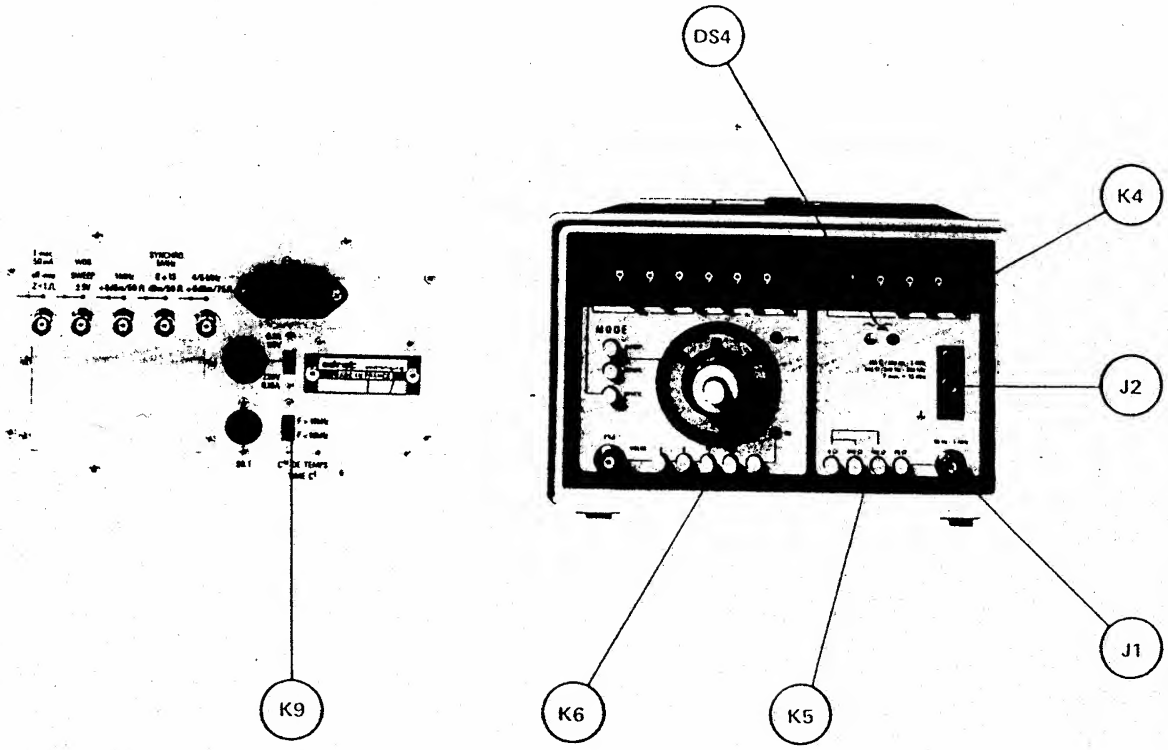
The usable frequency range goes from 200 Hz to 300 kHz, while the electromotive force ranges from 6.92 Vrms (+ 13 dBm/600 Ω display) to 490 µVrms (- 69.99 dBm/600 Ω display) in 0.01 dB steps.

IV-5 SQUARE-WAVE OUTPUT

Coaxial connector (J3) delivers a square wave with the same frequency as the main output signal and with 0 V, 5 V or 10 V amplitude selected on keyboard (K7). The "low" level of this square wave is 0V, which makes it compatible with TTL and C-MOS logical circuits.

IV-6 TRACKING OUTPUT

Coaxial connector (J4) permanently delivers a sinusoidal signal with + 6 dBm/75 Ω output level and 4 MHz frequency offset from the main output signal.



- Select the output impedance through keyboard **K5**. The output signal is delivered on connector **J1** for the 75 Ω impedance and on connector **J2** for the other impedances.
- In Local mode, set switch **K9** to **F < 10 kHz.**
- Adjust the output level through switches **K4**, the sign display being provided by indicator lights **DS4.**
- For suppressing the output signal without switching off the instrument, press key **K6.**

Figure IV-3 MAIN OUTPUT

IV-7 Z < 1 Ω AUXILIARY OUTPUT

A sinusoidal signal with less than 1 Ω output impedance and with the same frequency as the main output signal is available on coaxial connector (J8).

When the level setting of switches (K4) ranges from + 0 dBm to + 19.99 dBm, the electromotive force of this signal is equal to the level of the main output signal expressed in dBm/75 Ω.

When the level setting of switches (K4) ranges from - 0 dBm to - 69.99 dBm, the electromotive force varies from + 10 dBm/75 Ω to + 0.01 dBm/75 Ω according to the table below.

Setting of switches K4	- 0,00	- 9,99	- 10,00	- 19,99	- 20,00	- 29,99	- 30,00	- 39,99	- 40,00	- 49,99	- 50,00	- 59,99	- 60,00	- 69,99
Electromotive force in dBm/75 Ω	+ 10 ↘	+ 0,01	+ 10 ↘	+ 0,01	+ 10 ↘	+ 0,01	+ 10 ↘	+ 0,01	+ 10 ↘	+ 0,01	+ 10 ↘	+ 0,01	+ 10 ↘	+ 0,01

IV-8 ALC TIME CONSTANT

In order to optimize the output level settling time, this instrument is endowed with two ALC time constants selected through rear-panel switch (K9). The longer time constant provides level regulation over the entire frequency range (F < 10 kHz setting), whereas the other is reserved for frequencies higher than 10 kHz (F > 10 kHz setting).

In Local mode, it is well-advised to always set switch (K9) to the F < 10 kHz setting, which allows operation with any output frequency.

IV-9 OUTPUT LEVEL INHIBITION

Pressing front-panel key (K6) permits to suppress the main output signal, the Z < 1 auxiliary output signal and the square-wave signal without switching off the instrument.

IV-10 REFERENCE FREQUENCY

The 1 MHz reference frequency derived from the internal crystal oscillator is permanently available on connector (J6) with approximately 500 mVrms/50 Ω output level.

This internal crystal oscillator can be synchronized to a 5 MHz external reference signal applied to connector (J5) with 220 mVrms to 1 Vrms/50 Ω input level. In that case, the frequency delivered by the various outputs of the synthesizer has the stability of the reference frequency applied to connector (J5).

IV-11 SUPPLY VOLTAGES OUTPUT

Socket (S01), whose pin assignment is indicated in figure IV-4, provides + 12 V, + 6 V and - 12 V regulated voltages destined to external circuits.

Maximum current for each voltage : 100 mA.

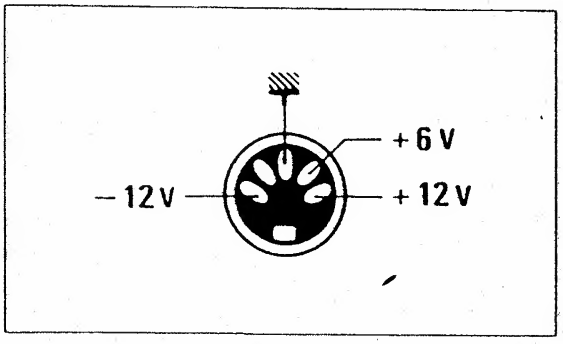


Figure IV-4 SOCKET (S01)

IV-12 PARALLEL BCD PROGRAMMING (OPTION 010)

Selection of the remote programming mode is achieved by applying a "0" logic level to pin 17 of connector (S03), which lights up indicator (DS2). All manual controls are then inhibited, save on/off switch (K1), impedance selection keyboard (K5), square-wave selection keyboard (K7), and mains voltage selector (K8).

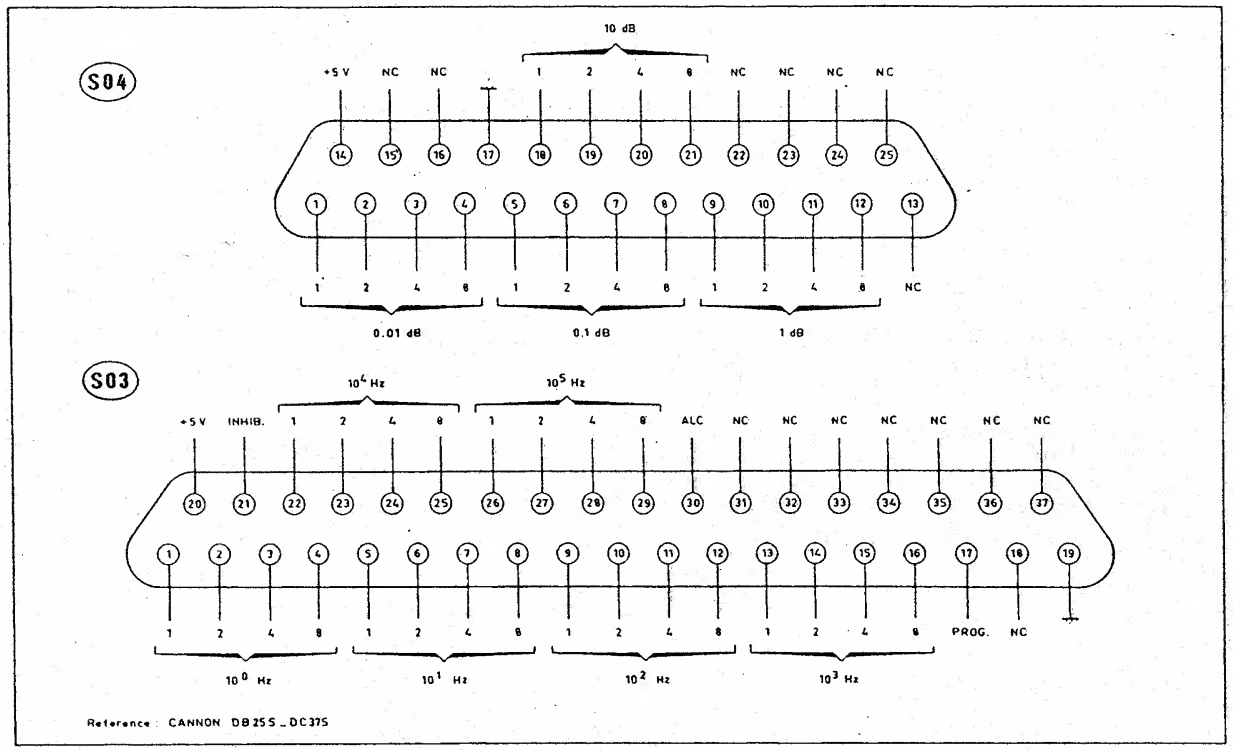


Figure IV-5 PARALLEL BCD PROGRAMMING CONNECTORS

The synthesized frequency programming is achieved in positive logic through TTL compatible signals applied to connector (S03) whose pin assignment is indicated in figure IV-5.

The output level is determined by programming the attenuation with respect to + 20 dBm. This attenuation programming is achieved in positive logic through TTL compatible signals applied to connector (S04). For instance, programming 9.32 dB provides + 10.68 dBm output level to the main signal.

The output level inhibition is obtained by applying a "0" logic level to pin 21 of connector (S03).

The ALC time constant programming is performed on pin 30 of connector (S03), a "0" logic level corresponding to F < 10 kHz and a "1" logic level corresponding to F > 10 kHz. The F < 10 kHz time constant may be selected with any output frequency, whereas the F > 10 kHz time constant is destined to the fast level switching of frequencies above 10 kHz.

Pin 20 of connector (S03) and pin 14 of connector (S04) continuously provide a + 5 V regulated voltage which can facilitate programming and be used as a pilot of the instrument operation (50 mA maximum current).

The input circuit of the programming signals consists of a 40097 buffer preceded with a 1N 4448 diode as shown in figure IV-6.

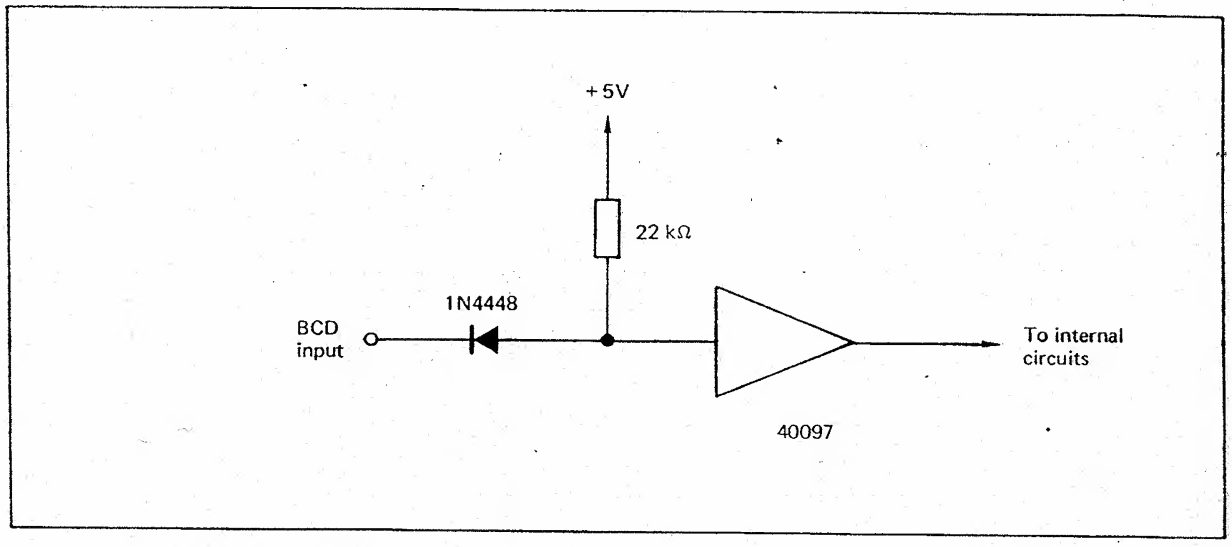


Figure IV-6 PROGRAMMING SIGNALS INPUT CIRCUIT

IV-13 IEEE BUS PROGRAMMING (OPTION 020)

The synthesizer programming through the IEEE bus is achieved in accordance with IEEE standard 488-1975 on connector (S05) whose pin assignment is indicated in figure IV-7.

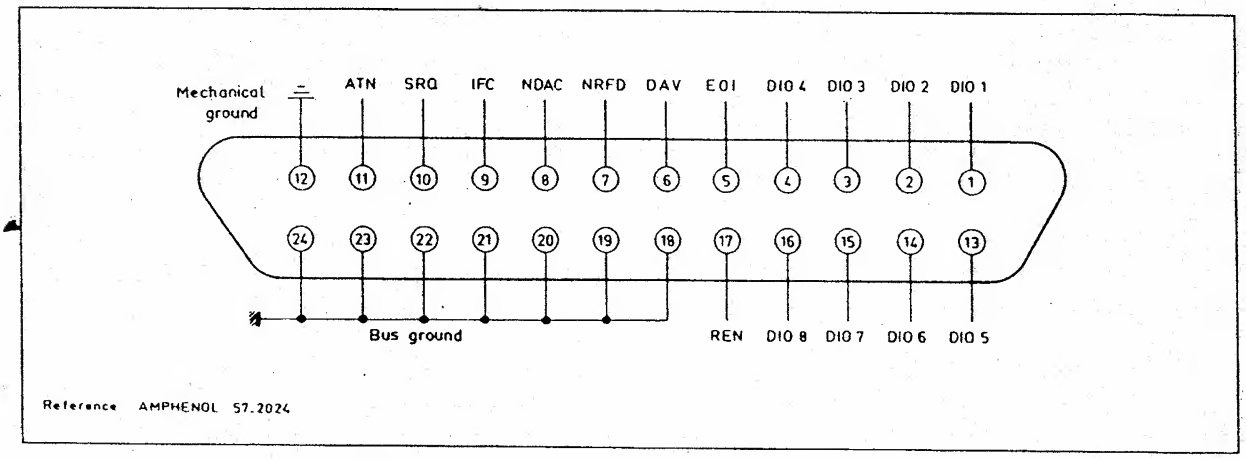


Figure IV-7 IEEE BUS CONNECTOR

IV-13-1 ADDRESSING

The instrument address is selected in binary code among numbers 0 to 30 through five digital switches (K10). This address is enabled by setting digital switch (K11) to "Addressable".

When switch (K11) is set to "Listen only", the instrument operates in continuous addressing.

Immediately after being addressed, the instrument goes to remote programming mode, which lights up indicator (DS2). The return to Local mode requires either reception of the GTL order (Go To Local), presence of a "1" logic level on line REN, or presence of a "0" logic level on line IFC.

In remote programming mode, all manual controls are inhibited, save on/off switch (K1), impedance selection keyboard (K5), square-wave selection keyboard (K7), and mains voltage selector (K8).

IV-13-2 FREQUENCY PROGRAMMING

The synthesized frequency programming is achieved by sending letter F followed with a whole number representing the frequency in Hz. If the transmitted number comprises a point, a comma, or more generally any character other than a figure, the figures sent after this character are ignored. This particularly prohibits the use of the floating point format.

Several characters may be inserted between letter F and the number representing the synthesized frequency. These characters are ignored by the instrument, provided that they are neither letter A, order CR (Carriage Return), or one of signs < and > .

IV-13-3 ALC TIME CONSTANT PROGRAMMING

Changing the ALC time constant is achieved by inserting sign < or > between letter F and the number representing the synthesized frequency, the < sign corresponding to F < 10 kHz and the > sign corresponding to F > 10 kHz. Without sign < or > inserted between letter F and the number representing the synthesized frequency, the ALC time constant remains unchanged.

The F < 10 kHz time constant may be selected with any output frequency, whereas the F > 10 kHz time constant is destined to the fast level switching of frequencies above 10 kHz.

IV-13-4 OUTPUT LEVEL PROGRAMMING

The output level is determined by programming the attenuation with respect to + 20 dBm. This attenuation programming is achieved by sending letter A followed with a whole number representing the attenuation in mB (0.01 dB). If the transmitted number comprises a point, a comma, or more generally any character other than a figure, the figures sent after this character are ignored by the instrument.

Several characters may be inserted between letter A and the number representing the output level attenuation. These characters are ignored by the instrument, provided that they are neither letter F, order CR (Carriage Return), or question mark ? .

IV-13-5 INHIBITION PROGRAMMING

The output level inhibition is programmed by sending letter A followed with question mark ? . This inhibition ends as soon as another attenuation is programmed.

IV-13-6 DATA ENABLE

The data received by the synthesizer are taken into account only after reception of order CR (Carriage Return), often sent automatically by the calculator at the end of the message, or order GET (Group Executive Trigger) that permits to simultaneously enable the data received by several instruments.

Inversely, orders A and F may be cancelled by sending either order DCL (Device Clear) or order SDC (Selective Device Clear).

IV-13-7 PROGRAMMING EXAMPLES

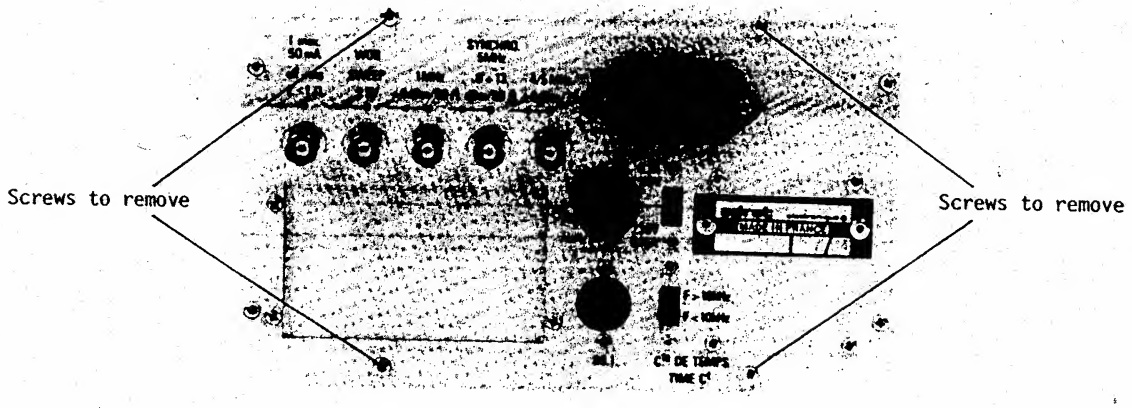
In the following examples, it is assumed that the instrument has been addressed and that the message ends by order CR (Carriage Return).

F < 1 9 7 8 A 0	Frequency 1978 Hz. Time constant F < 10 kHz. Level + 20 dBm.
F 2 0 0 0	Frequency 2000 Hz. Time constant unchanged. Level unchanged.
F R E Q U 5 2 5	Frequency 525 Hz (letters REQU and space are ignored). Time constant unchanged. Level unchanged.
F 1 5 0 0 . 3 5 F 1 5 0 0 , 3 5 F 1 5 0 0 3 5	Frequency 1500 Hz (the figures placed after the point, comma or space are ignored). Time constant unchanged. Level unchanged.
F > 5 9 2 8 1 A ?	Frequency 59281 Hz. Time constant F > 10 kHz. Level inhibition.
A 9 5 1	Frequency unchanged. Time constant unchanged. Level + 10.49 dBm (9.51 dB attenuation).
A T T E N . 9 5 1	Frequency unchanged. Time constant unchanged. Level + 10.49 dBm (letters TTEN and point are ignored).
A 9 5 1 . 2 5 A 9 5 1 , 2 5 A 9 5 1 2 5	Frequency unchanged. Time constant unchanged. Level + 10.49 dBm (the figures placed after the point, comma or space are ignored).
F < 5 0 0 0 A T T E N 9 5 1	Frequency 5000 Hz. Time constant F < 10 kHz. Level 10.49 dBm (letters TTEN are ignored).
F A 1 0 0 0	Frequency 1000 Hz. Time constant unchanged. Level + 10 dBm (10.00 dB attenuation).

IV-14 ADAPTATION TO 19" RACK

The synthesizer 2230 A can be incorporated in a 19" rack with the help of a cabinet reference 01 22309001 for the incorporation of one instrument, or reference 01 22309002 for the incorporation of two instruments. The procedure for inserting the 2230 A in either of these cabinets is as follows.

- Remove the four rear-panel screws holding the top and bottom covers.



- Pull out these two covers.
- Take off the top-cover handle (four screws to remove).
- Take off the four foots of the bottom cover.
- Set the covers back in their place without fixing them.
- Insert the 2230 A in the cabinet and screw back the four rear-panel screws.

APPENDIX

CHART OF ASCII CHARACTERS

BITS				b_7 b_6 b_5	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
b_4	b_3	b_2	b_1	Row \ Column	0	1	2	3	4	5	6	7
0	0	0	0	0	NUL	DLE		0	@	P	`	p
0	0	0	1	1	SOH	DC1	!	1	A	Q	a	q
0	0	1	0	2	STX	DC2	"	2	B	R	b	r
0	0	1	1	3	ETX	DC3	#	3	C	S	c	s
0	1	0	0	4	EOT	DC4	$	4	D	T	d	t
0	1	0	1	5	ENQ	NAK	%	5	E	U	e	u
0	1	1	0	6	ACK	SYN	&	6	F	V	f	v
0	1	1	1	7	BEL	ETB	'	7	G	W	g	w
1	0	0	0	8	BS	CAN	(	8	H	X	h	x
1	0	0	1	9	HT	EM	)	9	I	Y	i	y
1	0	1	0	10	LF	SUB	*	:	J	Z	j	z
1	0	1	1	11	VT	ESC	+	;	K	[	k	{
1	1	0	0	12	FF	FS	,	<	L	\	l	:
1	1	0	1	13	CR	GS	-	=	M	]	m	}
1	1	1	0	14	SO	RS	.	>	N	^	n	~
1	1	1	1	15	SI	US	/	?	O	—	o	DEL

IEEE BUS PROGRAMMING WITH CALCULATOR HP 9825A

```
0: "2230A programming with calculatcr HP9825":
1: "the instrument address is assumed to be 0":
2:
3: fmt 2f.0
4: ent "Frequency in Hertz",F
5: if F<10 or F>=1e6;dsp "Frequency out of range";gto "stop"
6: ent "Level in dBm",A
7: if A>20 or A<=-70;dsp "Level out of range";gto "stop"
8: if F<1e4;wrt 700,"F<",F,"A",2000-100*A;gto 4
9: wrt 700,"F>",F,"A",2000-100*A;gto 4
10: "stop":wrt 700,"A?";wait 1000;gto 4
11: end
```

CHAPTER V

CIRCUIT DESCRIPTION

V-1 INTRODUCTION

In all the schematics and figures of the present manual, the various circuits making up the instrument are designated by the following abbreviations :

A	Amplifier, buffer or shaper
CP	Phase comparator
D	Frequency divider
DP	Programmable frequency divider
DT	Level detector
FL	Filter
M	Mixer
O	Oscillator

V-2 GENERATION 10^0 Hz - 10^1 Hz - 10^2 Hz

Refer to block diagram in plate V-1 and figure V-1, and schematic in plate V-2.

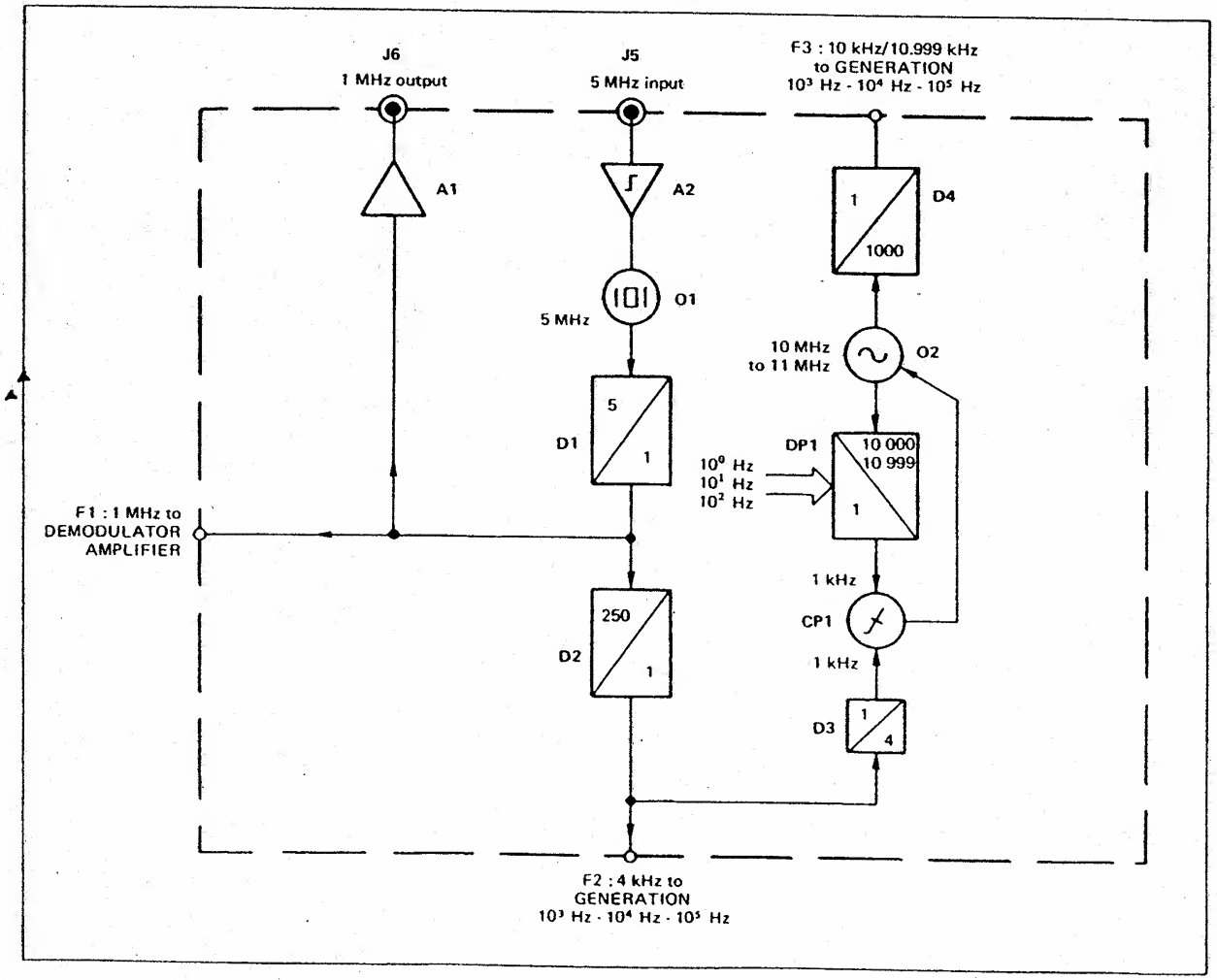


Figure V-1 GENERATION 10^0 Hz - 10^1 Hz - 10^2 Hz

This subassembly includes a phase-locked loop generating the 10^0 Hz, 10^1 Hz and 10^2 Hz increments of the output frequency, and the synthesizer time base.

The time base comprises crystal oscillator O2 which may be synchronized on an external 5 MHz frequency reference with 0 dBm to + 13 dBm/50 Ω input level thanks to shaper A2. The 5 MHz output frequency of oscillator O1 is divided by 5 in divider O1 in order to provide frequency F1 : 1 MHz required by the Demodulator Amplifier, and available on connector (J6) at a level of about + 6 dBm/50 Ω after amplification by A1. This frequency is then divided by 250 in divider D2 which delivers frequency F2 : 4 kHz to the Generation 10^3 Hz - 10^4 Hz - 10^5 Hz subassembly.

The phase-locked loop generating the 10^0 Hz, 10^1 Hz and 10^2 Hz increments of the output frequency includes oscillator O2, programmable counter DP1 and phase comparator CP1. Oscillator O1 generates a 10 MHz to 10.999 MHz frequency which is divided by the division rate N : 10 000 to 10 999 of programmable counter DP1. The output frequency of counter DP1 is then compared in phase comparator CP1 with a 1 kHz reference obtained by dividing frequency F2 : 4 kHz by 4 in divider D3. Phase comparator CP1 therefore provides a DC voltage which locks oscillator O1 onto a frequency equal to N times the reference frequency of 1 kHz.

The frequency generated by oscillator O1 is divided by 1000 in divider D4, which provides frequency F3 : 10 kHz/10.999 kHz routed to the Generation 10^3 Hz - 10^4 Hz - 10^5 Hz subassembly.

PRINCIPLE OF PROGRAMMABLE COUNTER DP1

Programmable counter DP1 includes two dividers with a division rate of 10 or 11, a divider with a division rate of 100 to 109, and two binary module comparators controlling respective dividers by 10 or 11.

During a count cycle, the front divider divides P times by 11, where P is the value of the 10^0 Hz digit programmed in positive logic on the corresponding binary module comparator (integrated circuit SN 16, plate V-2). During the remainder of the cycle, the division rate of this divider is equal to 10.

Similarly, the second divider by 10 or 11 divides Q times by 11 during each count cycle, where Q is the value of the 10^1 Hz digit programmed in positive logic on the binary module comparator SN17.

The divider by 100 to 109 is directly programmed in positive logic by the value R of the 10^2 Hz digit, its division rate being at all times equal to (100+R). The division rate N of programmable counter DP1 can thus be expressed as a function of P, Q and R as follows :

$$N = 10\left[11Q + 10\,(100 + R - Q) - P\right] + 11P$$

P, Q, R : 0 to 9

For example, if the programmed frequency is of the form --- 573 Hz, the front divider divides 3 times by 11 and 1054 times by 10. The second divider by 10 or 11 divides 7 times by 11 and 98 times by 10, while the divider by 100 to 109 continuously divides by 105. The division rate N is thus equal to 10573.

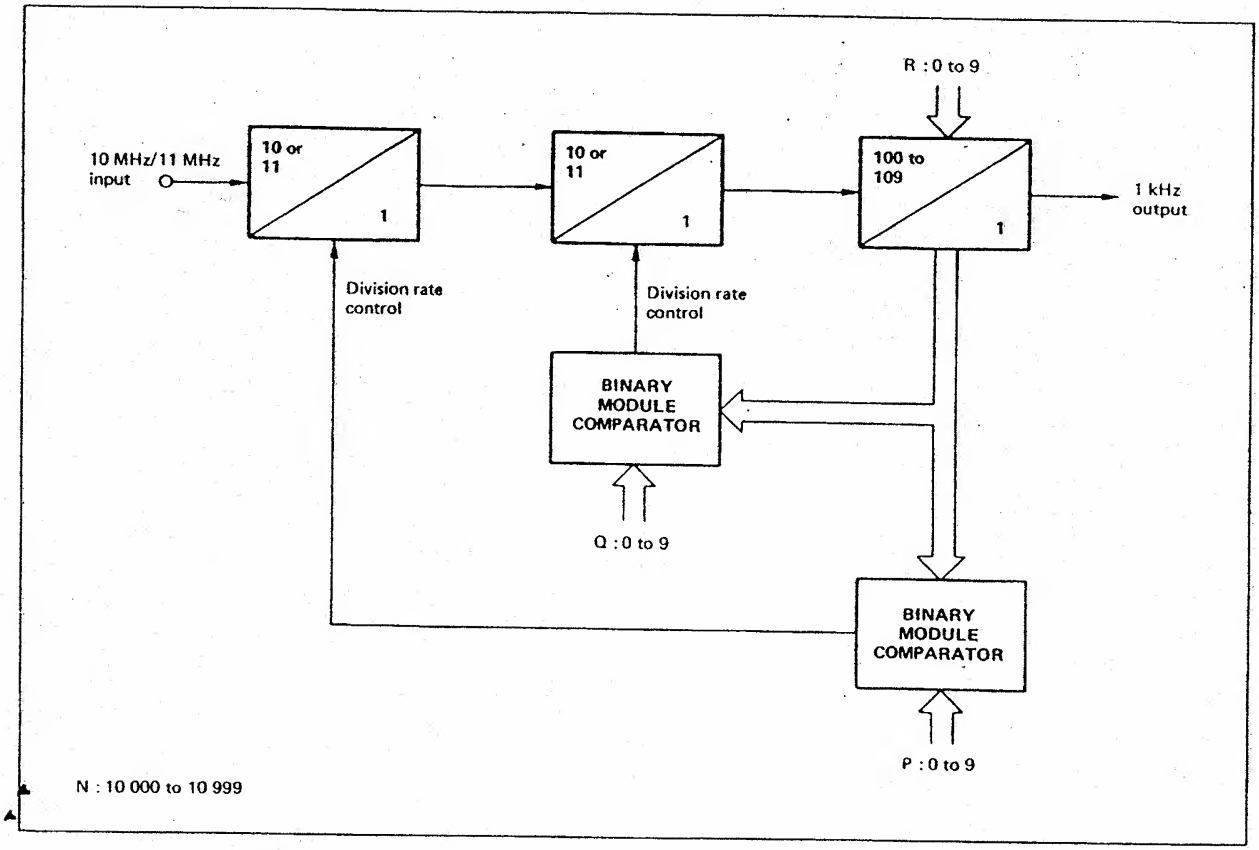


Figure V-2 PRINCIPLE OF COUNTER DP1

The front divider consists of a divider by 4 (integrated circuit SN11, plate V-2) preceded with a divider by 2 or 3 (integrated circuit SN10) whose division rate is controlled by two NAND gates (integrated circuit SN14). Depending on whether the whole must divide by 10 or 11, the sequence of division rates will be either 2 + 3 + 2 + 3 or 3 + 3 + 2 + 3.

The second divider by 10 or 11 is made up of integrated circuits SN12, SN13 and SN15, and operates on the same principle.

The divider by 100 to 109 consists of a BCD counter (integrated circuit SN18) followed by a binary counter (integrated circuit SN19). Inputs D8-D4-D2-D1 of the binary counter are continuously at state 1010, whereas those of the BCD counter receive the programming signals for the 10^2 Hz digit, which produces a division rate equal to (100 + R).

PHASE COMPARATOR PRINCIPLE

The operation of the phase comparator rests up on the generation of a sawtooth which is interrupted by a sampling pulse, as shown in figure V-3.

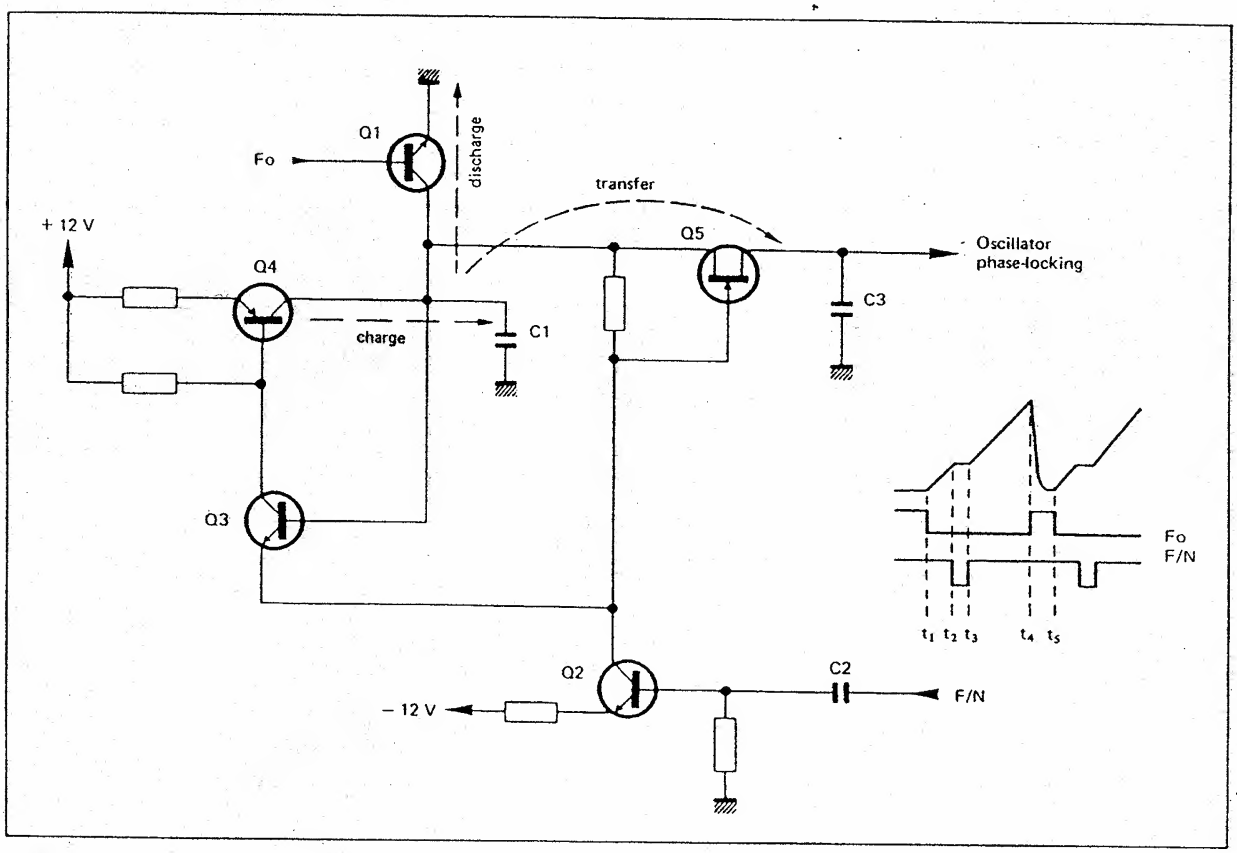


Figure V-3 PRINCIPLE OF PHASE COMPARATOR

At time t_1, the negative edge of the reference F_o cuts off transistor Q1, which starts the sawtooth by enabling capacitor C1 to charge at constant current.

At time t_2, the sawtooth is interrupted by the negative edge of the signal F/N from the programmable counter, which cuts off transistors Q2, Q3 and Q4. At the same time, field-effect transistor Q5 starts to conduct and transfers the charge from capacitor C1 to storage capacitor C3.

At time t_3, field-effect transistor Q5 is again cut off, whereas transistors Q2, Q3 and Q4 begin to conduct again, which restarts the sawtooth.

At time t_4, the positive edge of the reference signal F_o saturates transistor Q1 which therefore discharges capacitor C1. Another sawtooth begins at time t_5 on the negative edge of signal F_o.

Any relative phase shift affecting signals F_o and F/N shifts the time interval $(t_3 - t_2)$ towards time t_1 or time t_4. This displacement modifies the DC voltage stored in capacitor C3, which enables the frequency of the controlled oscillator to be corrected.

V-3 GENERATION 10^3 Hz - 10^4 Hz - 10^5 Hz

Refer to block diagram in plate V-1 and figure V-4, and schematic in plate V-3.

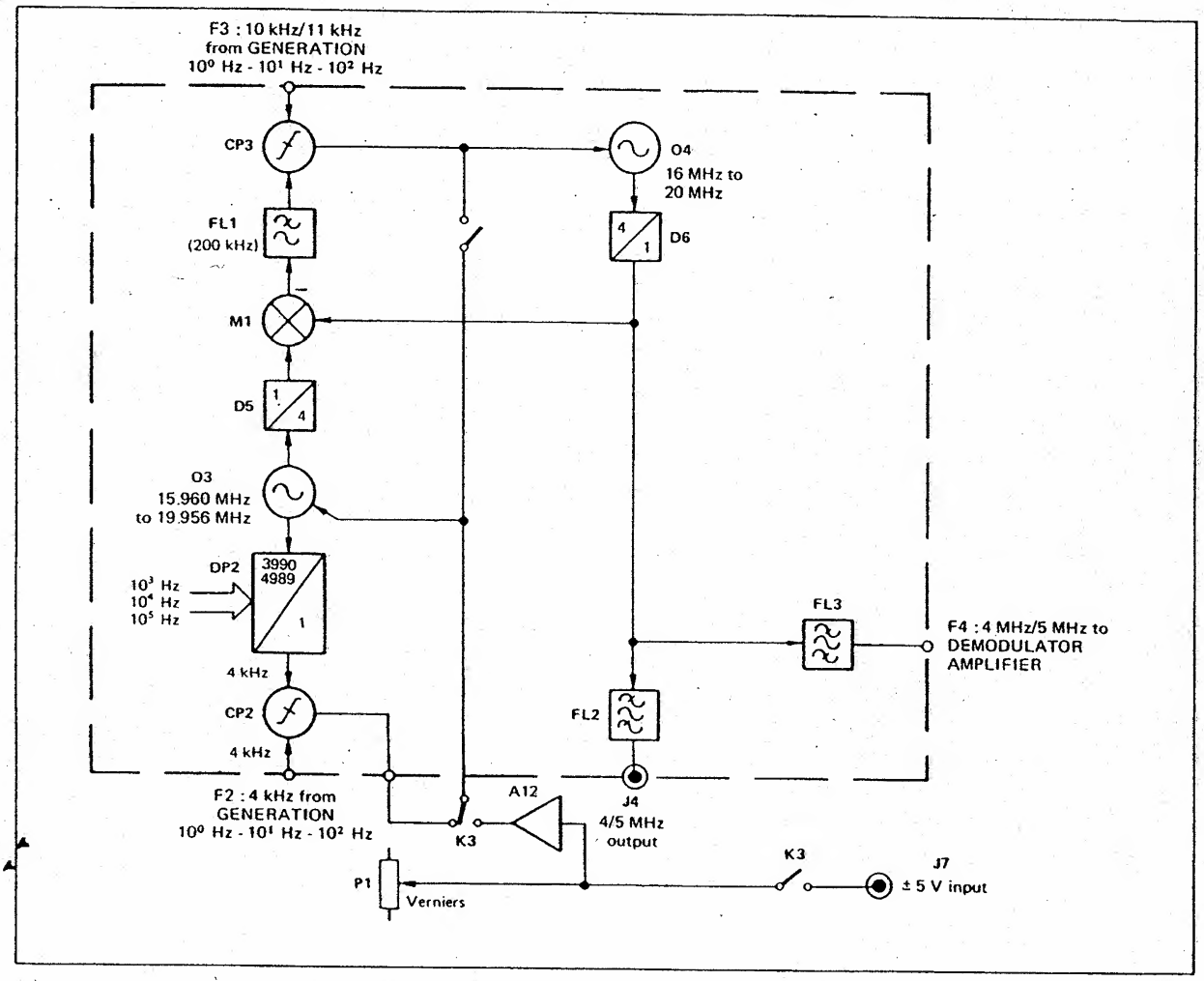


Figure V-4 GENERATION 10^3 Hz - 10^4 Hz - 10^5 Hz

This subassembly generates the 10^3 Hz, 10^4 Hz and 10^5 Hz increments of the output frequency while incorporating the 10^0 Hz, 10^1 Hz and 10^2 Hz increments carried by frequency F3 : 10 kHz/10.999kHz obtained at the output of the previously described subassembly.

The 10^3 Hz, 10^4 Hz and 10^5 Hz increments are generated by means of a phase-locked loop comprising oscillator O3, programmable counter DP2 and phase/frequency comparator CP2. Oscillator O3 delivers a frequency between 15.960 MHz and 19.956 MHz, that is divided by N : 3990 to 4989 in programmable counter DP2. The output frequency of counter DP2 is then compared in phase/frequency comparator CP2 with the reference frequency F2 : 4 kHz coming from Generation 10^0 Hz - 10^1 Hz - 10^2 Hz. In Synthesizer mode, comparator CP2 thus provides a DC voltage locking oscillator O3 onto a frequency equal to N times the reference frequency F2 : 4 kHz. In Generator or Sweeper mode, this control voltage is replaced by the output voltage of amplifier A12 (Control Circuits, plate V-7) providing for gradual variation of the output frequency of oscillator O3.

The combination of the 10^0 Hz, 10^1 Hz and 10^2 Hz increments carried by frequency F3 and the 10^3 Hz, 10^4 Hz and 10^5 Hz increments generated by oscillator O3 is effected by means of a second phase-locked loop comprising oscillator O4, divider D6, mixer M1, filter FL1 and phase/frequency comparator CP3.

Oscillator O4 delivers a frequency variable from 16 MHz to 20 MHz, that divider D6 divides by 4 in order to provide a 4 MHz to 5 MHz frequency. Mixer M1, made of an exclusive OR gate, beats this frequency with a 3.990MHz to 4.989MHz signal obtained by dividing the output frequency of oscillator O3 by 4 in divider D5.

Low-pass filter FL1 selects the difference frequency, and outputs a signal at a frequency variable between 10 kHz and 10.999 kHz, which is then compared in phase/frequency comparator CP3 with frequency F3 : 10 kHz/10.999 kHz coming from the Generation 10^0 Hz - 10^1 Hz - 10^2 Hz subassembly. Comparator CP3 therefore supplies a DC voltage which locks oscillator O4 onto a frequency comprising the 10^0 Hz to 10^2 Hz increments and also the 10^3 Hz to 10^5 Hz increments. In order to prevent oscillator O4 from locking onto a frequency below that generated by oscillator O3, mixer M1 and low-pass filter FL1 provide a signal in phase quadrature with the frequency to be compared. This signal is applied to the J input of one of the flip-flops of comparator CP3, and disables the phase comparison if the output frequency of divider D6 is less than that of divider D5.

The output signal of divider D6 is converted to a sinusoidal signal by band-pass filters FL2 and FL3, which respectively deliver frequency F4 : 4 MHz/5 MHz to connector (J4) on the rear panel of the instrument and to the Demodulator Amplifier subassembly.

During frequency changes involving the 10^3 Hz, 10^4 Hz or 10^5 Hz increments, an electronic switch consisting of transistors Q12 and Q13 (plate V-3) replaces the control voltage from comparator CP3 with an approach voltage obtained from comparator CP2 (Synthesizer mode) or from amplifier A12 (Generator or Sweeper mode). This substitution is intended to bring the output frequency of oscillator O4 close to its final value and is carried out when the difference between the control voltage and the approach voltage exceeds 0.6 volts.

PRINCIPLE OF PROGRAMMABLE COUNTER DP2

Programmable counter DP2 basically comprises two dividers by 10 or 11, a divider by 39 to 49, two BCD adders and two binary module comparators controlling respective dividers by 10 or 11.

During a count cycle, the front divider divides P times by 11, where P is the value of the 10^3 Hz digit programmed in positive logic on the corresponding binary module comparator (integrated circuit SN7, plate V-3). During the remainder of the cycle, the division rate of this divider is equal to 10.

The second divider by 10 or 11 divides Q times by 11 during each count cycle, where Q is the value of the 10^4 Hz digit shifted by 9. This shift is carried out by means of a BCD adder (integrated circuit SN11) whose inputs B8 - B4 - B2 - B1 are set to state 1001, while the inputs A8 - A4 - A2 - A1 receive the BCD programming signals of the 10^4 Hz digit.

For example, if the 10^4 Hz digit is 3, the BCD adder carries out the operation 9 + 3 = 12, and the binary module comparator SN8 receives the digit Q = 2, which gives a division rate of 11 twice per cycle.

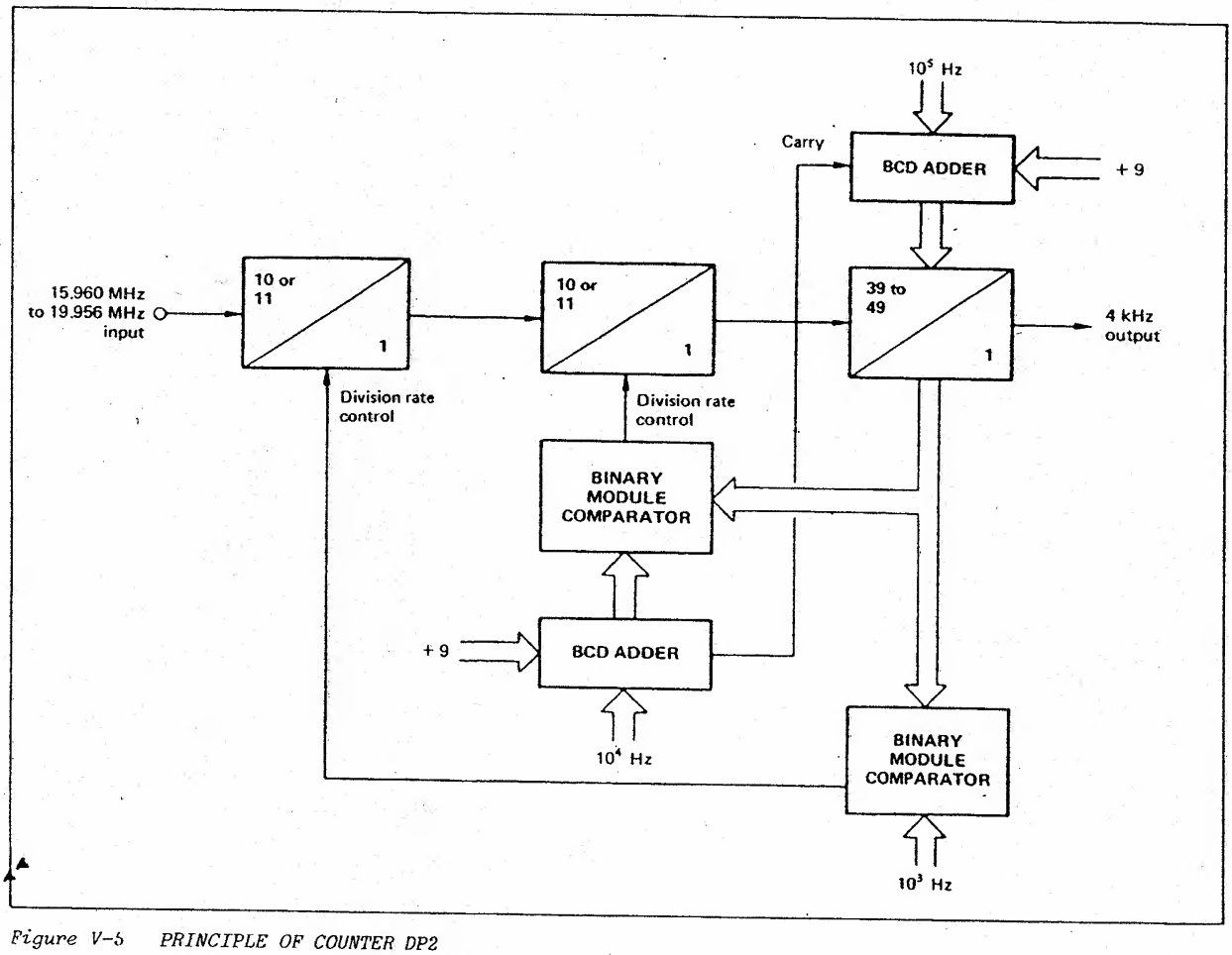


Figure V-5 PRINCIPLE OF COUNTER DP2

The divider by 39 to 49 is directly programmed in positive logic by the value R of the 10^5 Hz digit shifted by 9 or 10. As before, this shift is effected by means of a BCD adder (integrated circuit SN12) whose inputs B8 - B4 - B2 - B1 are set to state 1001. The input Cin receives the carry from adder SN11, and inputs A8 - A4 - A2 - A1 receive the programming signals of the 10^5 Hz digit. For example, if the 10^5 Hz and 10^4 Hz digits are respectively 5 and 3, the BCD adder achieves the operation 9 + 5 + carry = 15, and the counter by 39 to 49 receives the digit R = 5, which gives a division rate of 39 + R = 44.

The front divider consists of a divider by 4 (integrated circuit SN5) preceded with a divider by 2 or 3, the division rate of which is controlled by two NAND gates (integrated circuit SN5). Depending on whether the whole is to divide by 10 or 11, the sequence of division rates will be 2 + 3 + 2 + 3 or 3 + 3 + 2 + 3. The second divider by 10 or 11 comprises integrated circuits SN3, SN4 and SN6, and operates on the same principle.

The divider by 39 to 49 consists of a BCD counter (integrated circuit SN9) followed by a binary counter (integrated circuit SN10), whose inputs D8 - D4 - D2 - D1 receive the programming signals from adder SN12.

PRINCIPLE OF PHASE/FREQUENCY COMPARATOR

The operating principle of the phase/frequency comparator consists in generating pulses with a width proportional to the relative phase of the two compared signals, then in integrating these pulses so as to obtain a DC voltage permitting the phase-locking of an oscillator.

When the compared frequencies Fo and Fx are identical, the phase/frequency comparator acts as a phase comparator. When these two frequencies are unequal, the phase/frequency comparator indicates which one is larger, whence its appellation "phase/frequency comparator".

As shown in figure V-6,the digital section of the comparator consists of two J-K flip-flops whose outputs Q1 and Q2 are connected to an AND gate controlling the Reset input of each flip-flop.

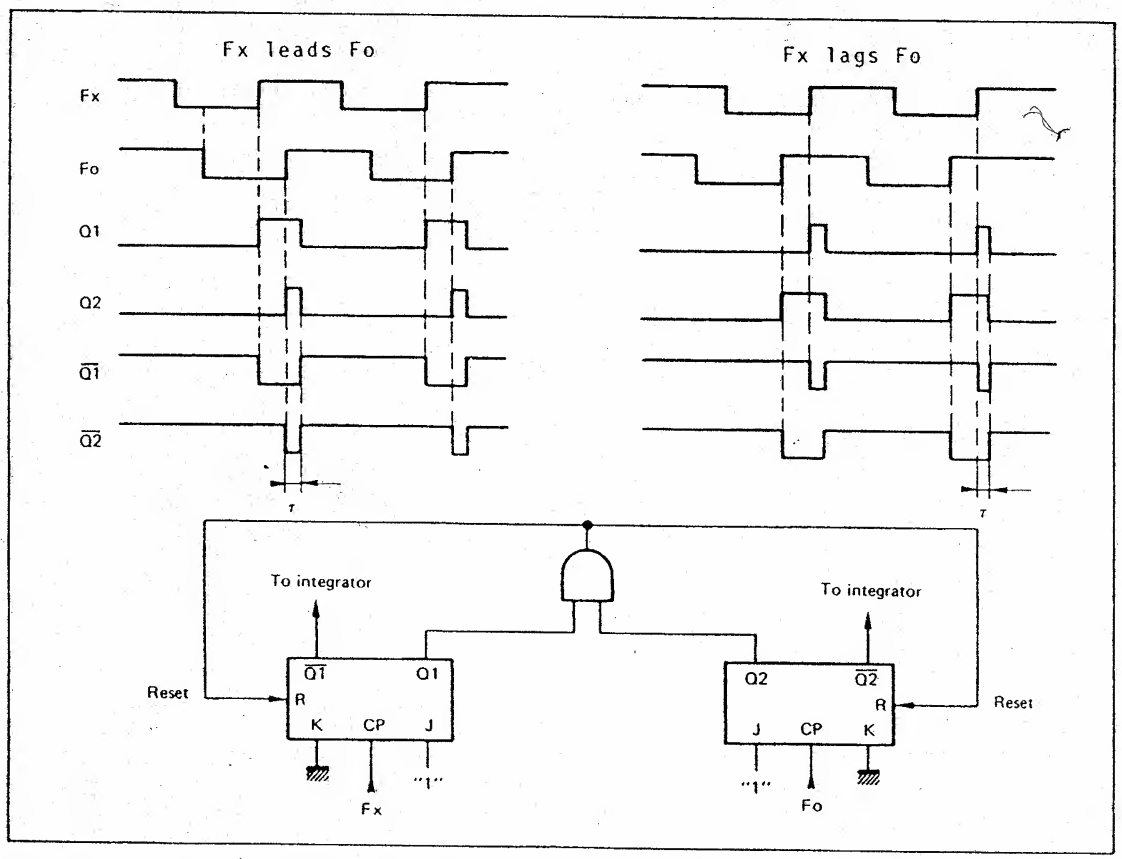


Figure V-6 PRINCIPLE OF PHASE/FREQUENCY COMPARATOR

The signals Fo and Fx to be compared are applied to the CP inputs of respective flip-flops. The K inputs are grounded and the J inputs receive a logic "1", so that the positive edges of the signals Fo and Fx cause a logic "1" to appear at the Q output of the corresponding flip-flop. Due to the reaction of the AND gate upon the Reset inputs, outputs Q1 and Q2 return to state "0" after they have both reached state "1", with a brief delay equal to the propagation time through the AND gate.

The difference between the widths of the pulses at outputs Q1 and Q2 is therefore proportional to the relative phase of the signals Fo and Fx. A DC voltage proportional to this relative phase is therefore obtained by integrating the output pulses by means of a differential integrator.

V-4 DEMODULATOR - AMPLIFIER

Refer to block diagram in plate V-1 and figure V-7, and schematic in plate V-4.

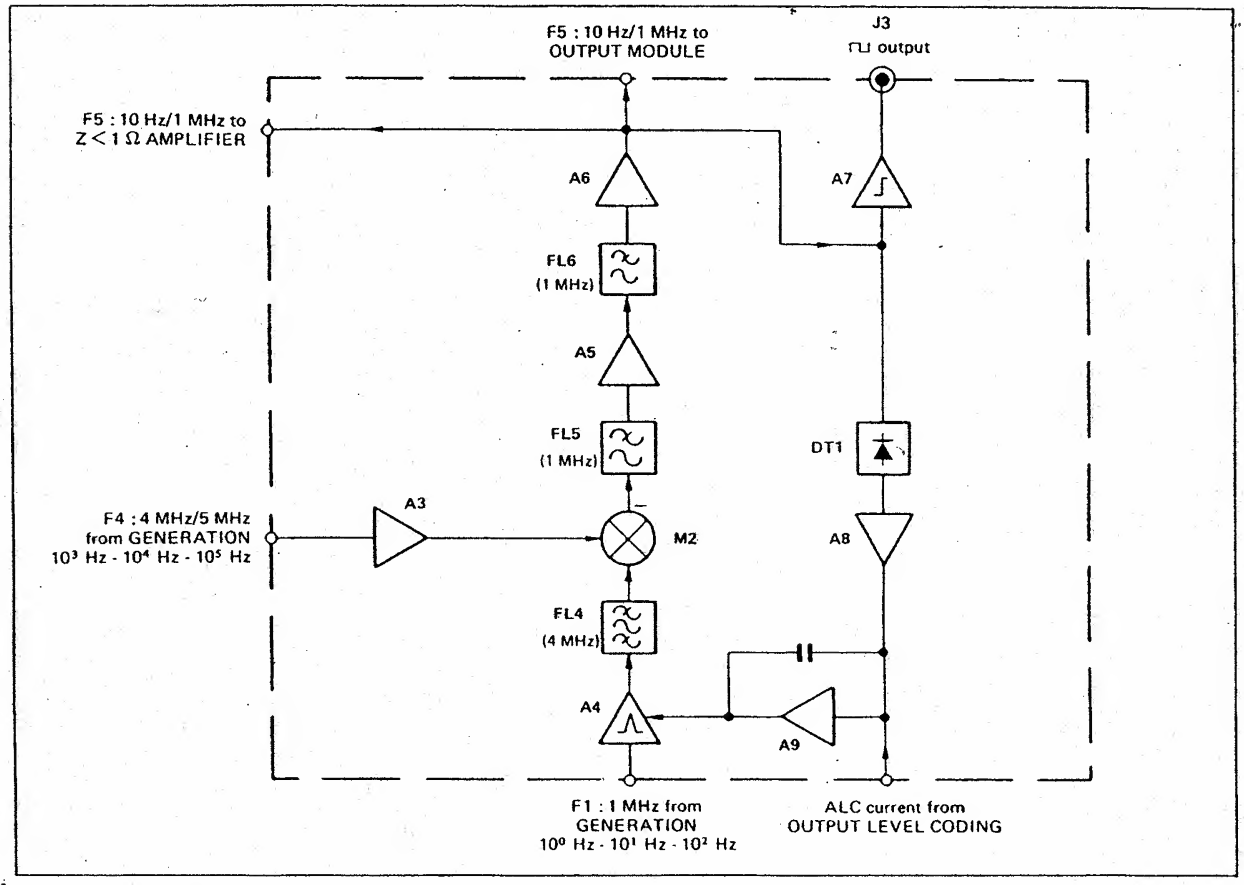


Figure V-7 DEMODULATOR - AMPLIFIER

The Demodulator Amplifier subassembly converts frequency F4, which is variable from 4 MHz to 5 MHz in steps of 1 Hz, to output frequency F5 : 10 Hz/1MHz and provides regulation of the output level.

Mixer M2 and low-pass filter FL5 carry out a substractive mixing of frequency F4 : 4 MHz/ 5 MHz coming from buffer A3 with a 4 MHz signal obtained by multiplying by 4 frequency F1 : 1 MHz issued from the Generation 10^0 Hz - 10^1 Hz - 10^3 Hz subassembly, this frequency multiplication being carried out by harmonic generator A4 and band-pass filter FL4. Frequency F5 : 10 Hz/1MHz obtained at the output of low-pass filter FL5 is amplified by amplifier A5, filtered through low-pass filter FL6 and again amplified by amplifier A6, providing an output signal between 550 mVrms and 5.5 Vrms, depending on the level set on switches (K4). The output signal of amplifier A6 is routed to the Output Module, to Z < 1 Ω Amplifier, and to shaper A7 providing square-wave signals at an amplitude of 5 V or 10 V to connector (J3).

The level of the signal at the output of amplifier A6 is detected by means of a full-wave detector DT1 whose outputs are connected to differential amplifier A8. This provides an ALC current which, following integration in amplifier A9, regulates the level of the 4 MHz signal applied to mixer M2 and consequently the level of the output signal. In addition to the ALC current from amplifier A8, integrator A9 receives a current proportional to the 1 dB, 0.1dB and 0.01dB increments of the output level from the Output Level Coding subassembly.

The ALC time constant is controlled by the parallel connection of a 10 µF capacitor with the integrating capacitor of amplifier A9, which has a value of 0.1 µF . The parallel connection of the 10 µF capacitor provides a long ALC time constant enabling the output level to be regulated over the entire frequency range. On the other hand, the switching out of circuit of this capacitor provides for rapid switching of frequencies above 10 kHz.

The output level inhibition is obtained by cutting off transistor Q1, which disables integrator A9 and removes the 4 MHz signal from mixer M2.

V-5 OUTPUT LEVEL CODING

Refer to block diagram in plate V-1 and figure V-8, and schematic in plate V-5.

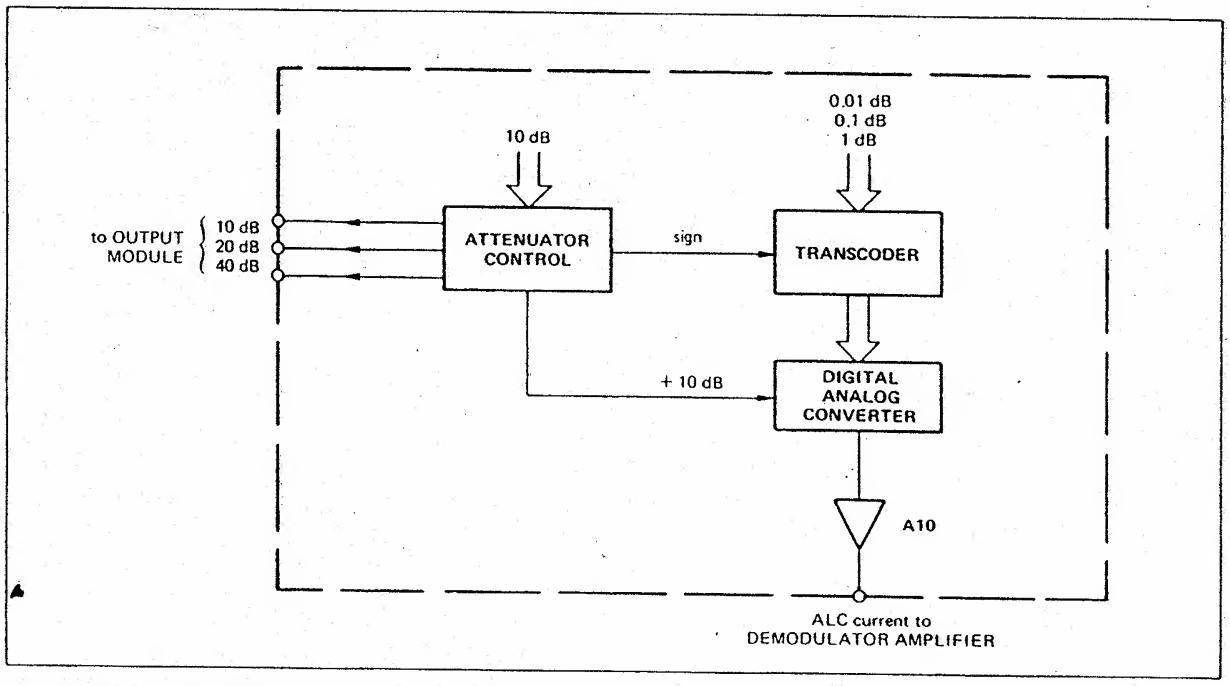


Figure V-8 OUTPUT LEVEL CODING

The Output Level Coding subassembly comprises attenuator control circuitry and a digital/analog converter which outputs a current proportionnal to the 1 dB, 0.1 dB and 0.01 dB increments of the output level.

The attenuator is controlled by means of a BCD/decimal decoder (integrated circuit SN1) and OR gates (integrated circuits SN2 and SN3) which switch the attenuating cells as a function of the output level 10 dB steps, as shown in the table of figure V-9. The signal obtained at output 0 of the BCD/decimal decoder is also sent to the digital/analog converter so as to increase by 10 dB the ALC current sent to the Demodulator Amplifier when the output level is between + 10 dBm + 20 dBm.

Setting of 10 dB steps	+ 10 dB ALC current	10 dB cell	20 dB cell	40 dB cell
+ 1	1	0	0	0
+ 0	0	0	0	0
- 0	0	1	0	0
- 1	0	0	1	0
- 2	0	1	1	0
- 3	0	0	0	1
- 4	0	1	0	1
- 5	0	0	1	1
- 6	0	1	1	1

Figure V-9 CODING OF 10-dB STEPS

The digital/analog converter comprises an operational amplifier (integrated circuit SN5) whose non-inverting input is connected to a resistor network switched by C-MOS switches (integrated circuits SN9 to SN13). The switching operation is controlled by a code converter consisting of three type 4561 integrated circuits providing a positive or negative count of the value of the 1 dB, 0.1 dB and 0.01 dB increments of the output level. In local mode between + 0 dBm and + 19.99 dBm, this value is counted in the positive sense, the type 4561 integrated circuits providing the 9's complement of the input signals. In local mode between - 0 dBm and - 69.99 dBm, and in Remote programming mode, the type 4561 integrated circuits are transparent and the value of the 1 dB, 0.1 dB and 0.01 dB steps is counted negatively.

Depending on the state of the 0 output of the BCD/decimal decoder SN1, the analog signal obtained from operational amplifier SN5 is transmitted directly to follower amplifier A10, or is first attenuated by 10 dB by means of resistors R20 and R21. In both cases, follower amplifier A10 supplies to the Demodulator Amplifier a current which is proportional to the level of the signal at the output of amplifier A6.

V-6 OUTPUT MODULE

Refer to block diagram in plate V-1 and figure V-10, and schematic in plate V-6.

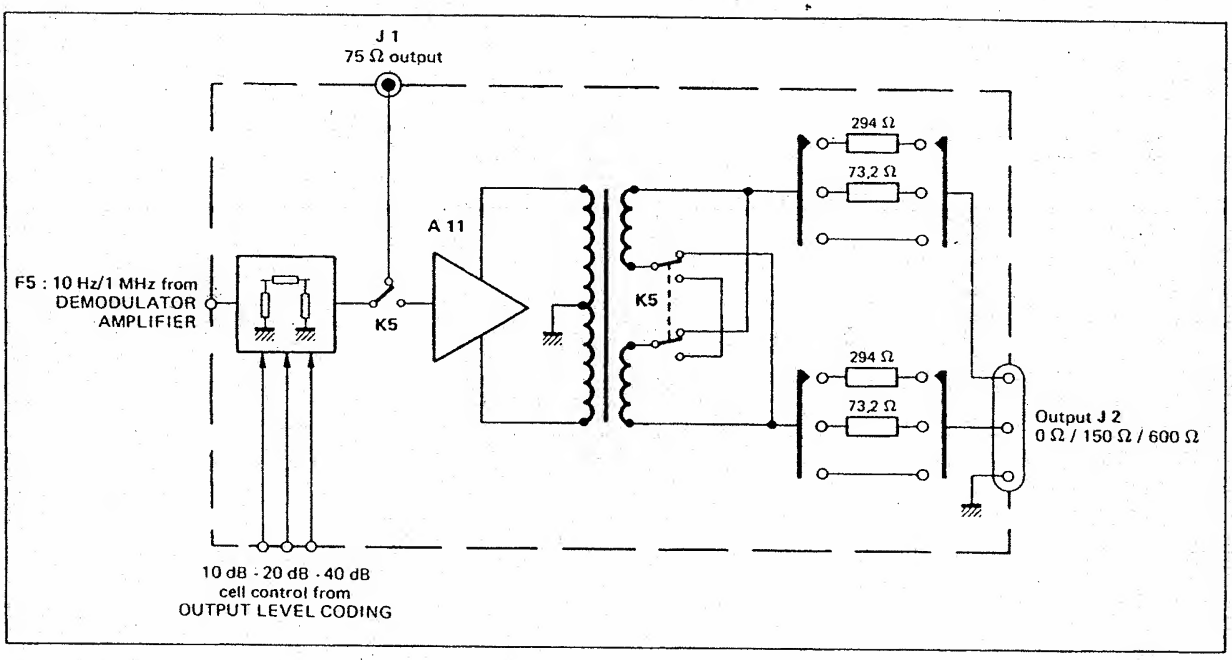


Figure V-10 OUTPUT MODULE

This module includes the output attenuator and the impedance converter circuit which enables the output signal of the synthesizer to be supplied at four different impedances.

The output attenuator includes three π cells with 75 Ω characteristic impedance providing respectively 10 dB, 20 dB and 40 dB attenuation. Each of these cells is controlled by means of a - 12 V voltage issued from the Output Level Coding subassembly.

The impedance converter circuit consists of symmetrical amplifier A11, a transformer with four windings, and impedance selection keyboard (K5). In order to avoid all risk of the transformer core saturating, amplifier A 11 has an automatic DC current centering circuit consisting of operational amplifier SN2.

When an impedance of 75 Ω is selected on keyboard (K5), the signal provided by the output attenuator is applied directly to connector (J1). For all other impedances, this signal is routed to amplifier A11 and the impedance converter before being applied to connector (J2).

When the "150 Ω" key of keyboard (K5) is pressed, the two secondary windings of the transformer are connected in parallel and two 73.2 Ω resistors are connected to the output. These resistors are short-circuited if the "0 Ω" key is also pressed. When the "600 Ω" key is pressed, the two secondary windings are connected in series and two resistors of 294 Ω are connected to the output, these resistors being short-circuited if the "0 Ω" key is also pressed.